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10/612,831	07/01/2003	Antonio Maria Borneo	851763.435	3911

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EXAMINER	
TECKLU, ISAAC TUKU	
ART UNIT	**PAPER NUMBER**
2192	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,831	BORNEO ET AL.	
	Examiner	Art Unit	
	Isaac T. Tecklu	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 26-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed on 11/27/2006.
2. Claims 1-14 have been amended.
3. Claims 23-25 have been cancelled.
4. New claims 26-27 have been added.
5. Claims 1-22 and 26-27 have been examined.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-11 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno et al. (US 5,951,674 B1) in view of Wong (US 6,988,183 B1).

As per claim 1 (Currently Amended), Moreno discloses process for executing programs on a multiprocessor system having a plurality of processors, having a given instruction set architecture (e.g. FIG. 6, element 606 and FIG. 16, element 706 and related text), each of said processors being able to execute, at each processing cycle, a respective maximum number of instructions (col. 9: 10-20 "... executed by a processor that accepts a maximum of six primitive operations per VLIW ..."), characterized in that it comprises the operations of:

compiling, at least in part, the instructions of said programs as instruction words of given length executable on a first processor of said plurality (col. 5: 45-50 " ... operation placed in a tree-instruction by a VLIW compiler ..." and FIG. 3 and related text); and

modifying, during runtime of one of said programs, at least some of said instruction words of given length of the one of said programs converting them into modified-instruction words executable on a second processor of said plurality (col. 10: 47-55 "... translation process .... "), said modification operation in turn having at least one operation selected from the group of:

splitting said instruction words into modified-instruction words (col. 10:45-50 " ... effectively splitting the tree into two ..." and e.g. FIG. 8 and 9 and related text); and

entering in the modified-instruction words no-operation instructions (col. 11:1-10 " ... by inserting an implicit unconditional branch to the next sequential chunk ...").

Moreno does not explicitly disclose modifying, during runtime of one of said programs. However, Wong discloses a device comprising an instruction stream transforming unit that transforms code blocks of instruction from an original instruction set architecture to a transformed instruction set architecture (e.g. Figure 6). The device performs transformation of instruction outside of the execute unit and the run-time execution process (col. 3: 12-17). The transformation is done by splitting of a hyper-block into two paths (col. 12: 25-30). Therefore it would have been obvious to one skilled in the art at the time of the invention was made to modify portion of the instruction at runtime to accelerate execution of a program by the processor by transforming portions of said program code at run-time into the transformed instruction set architecture for more efficient execution and caching the transformed code within the instruction stream cache for possible repeated execution without requiring repeated transformations as once suggested by Wong (col. 36:10-19).

As per claim 2 (Currently Amended), Moreno discloses the process according to claim 1, ~~characterized in that it comprises the operations of~~ further comprising:

compiling the instructions of said programs in part as first instruction words having a first given length and executable on said first processor of said plurality and in part as second instruction words of given length executable on a second processor of said plurality (col. 5: 45-50 " ... operation placed in a tree-instruction by a VLIW compiler ..." and FIG. 3 and related text);

modifying at least some of said first instruction words into first modified-instruction words executable on said second processor of said plurality (col. 9: 58-65 "... translated into VLIWs at I-cache reload time ..."); and

modifying at least some of said second instruction words into second modified-instruction words executable on said first processor of said plurality (col. 10:10-20 "... translated into variable-length VLIWs whose maximum size matches ...").

As per claim 3 (Currently Amended), Moreno discloses the process according to claim 2, ~~characterized in that~~ wherein said first instruction words and said second instruction words have, respectively, a first and a second maximum length with said first maximum length greater than said second maximum length (col.11: 45-60 "... maximum size of the variable length is four-way branch ..."), the quotient between said first maximum length and said second maximum length having a given value with the possible presence of a remainder (e.g. FIG. 3 and FIG. 4 and related text) and in that the procedure comprises the operations of:

modifying said first instruction words by having said first maximum length into first modified-instruction words having said second maximum length by (col. 9: 58-65 "... translated into VLIWs at I-cache reload time ..."):

splitting said first instruction words into a number of said first modified-instruction words equal to the value of said quotient (col. 10:45-50 " ... effectively splitting the tree into two ..." and e.g. FIG. 8 and 9 and related text); and

in the presence of said remainder, adding to said first modified-instruction words a further modified-instruction word of length equal to said second maximum length, said second maximum length being obtained by entering into said further first modified-instruction word a set of no-operation instructions (e.g. FIG. 11 and related text); and

modifying said second instruction words by having said second maximum length into second modified-instruction words having said first maximum length by (col. 10:10-20 "... translated into variable-length VLIWs whose maximum size matches ..."):

adding to said second instruction words of said second maximum length a number of no-operation instructions equal to the difference between said first maximum length and said second maximum length (e.g. FIG. 11 and related text).

As per claim 4 (Currently Amended), Moreno discloses the process according to claim 1 ~~characterized in that it comprises the operations of~~ further comprising:

encoding said instructions on a given number of bits, said number of bits having a first bit identifying a length of instruction word executable on a processor of said plurality (col. 10: 35-40 "... instructions are encoded ...");

associating to said given number of bits a respective appendix having a set of further bits identifying lengths of instruction words executable on different processors of said plurality (e.g. FIG. 6, element 612 and related text);

identifying for each of said instructions a processor of said plurality designed to execute said instruction, said identified processor being able to process for each processing cycle a given length of instruction word (col. 20: 55-60 "... instruction already identified ..."); and

entering in the position of said first identifier bit a chosen bit between said further bits of said appendix, said chosen bit identifying the length of instruction word that can be executed by said identified processor (e.g. FIG. 6, element 604 and related text).

As per claim 5 (Currently Amended), Moreno discloses the process according to claim 4, ~~characterized in that it comprises the operations of~~ further comprising the operation of erasing said respective appendix before execution of the instruction (e.g. FIG. 6, element 610 and related text).

As per claim 6 (Currently Amended), Moreno discloses the process according to claim 4, ~~characterized in that~~ wherein said chosen bit is entered in the position of said first identifier bit in a step chosen from among: decoding of the instruction in view of the execution; re-filling of the cache associated to said identified processor; and decompression of the instruction in view of the execution (col. 9: 5-20"... smaller trees would have to be filled with no-op operations ... ").

As per claim 7 (Currently Amended), Moreno discloses the process according to claim 1, ~~characterized in that it comprises the operations of~~ further comprising

alternatively distributing the execution of the instructions of said sequence between the processors of said plurality, said instructions being directly executable by the processors of said plurality in conditions of binary compatibility (e.g. FIG. 1, element 606 and related text).

As per claim 8 (Currently Amended), Moreno discloses the process according to claim 1, ~~characterized in that it comprises the operations of~~ further comprising the operation of selectively distributing the execution of said instructions among the processors of said plurality, distributing dynamically the computational load of said processors (e.g. FIG. 18 and related text).

As per claim 9 (Currently Amended), Moreno discloses the process according to claim 1, ~~characterized in that it comprises the operations of~~ further comprising the operation of selectively distributing the execution of said instructions between said processors of said plurality with the criterion of equalizing the operating frequency of the processors of said plurality (e.g. FIG. 18 and related text).

As per claim 10 (Currently Amended), Moreno discloses the process according to claim 1, ~~characterized in that it comprises the operations of~~ further comprising the operation of performing a control process executed by at least one of the processors of said plurality so as to equalize its own workload with respect to the other processors of said multiprocessor system (e.g. Fig. 5, element 12 and related text).

As per claim 11 (Currently Amended), Moreno discloses the process according to claim 1, ~~characterized in that it comprises the operations of~~ further comprising the operation of drawing up a table accessible by said control process, said table having items selected from the group of:

a list of processes being executed or suspended on any processor of said plurality of processors (e.g. FIG. 16 and related text);

the progressive number thereof according to the order of activation; the percentage of maximum power of the processor that is used by said process (e.g. FIG. 18 and related text);

the execution time, said time, if zero, indicating that the process is temporarily suspended from being executed (FIG. 8 and related text);

the amount of memory of the system used by the process to be able to execute the function for which it is responsible (FIG. 8 and related text);

the maximum length of the long instruction that the VLIW processor can execute and for which it had been generated during compiling (col. 10:10-20 "... translated into variable-length VLIWs whose maximum size matches ...");

maximum length of the long instruction of the VLIW processor on which it is executed (col. 9: 10-20 "... executed by a processor that accepts a maximum of six primitive operations per VLIW ..."); and

the address of the portion of memory in which the data and the instructions are stored (Fig. 5, element 503 and related text).

As per claim 26 (New), Moreno discloses the process according to claim 1, further comprising:

executing, by the second processor, the modified instruction words (col. 17:25-35 "... for execution by processor ...").

As per claim 27 (New), Moreno discloses the multiprocessor system according to claim 12 wherein said means for converting instruction words of the first length compiled for execution on the first processor into modified instruction words of the second length executable on the second processor comprises converting the instruction words during runtime.

Moreno does not explicitly disclose modifying, during runtime of one of said programs. However, Wong discloses a device comprising an instruction stream transforming unit that transforms code blocks of instruction from an original instruction set architecture to a transformed instruction set architecture (e.g. Figure 6). The device performs transformation of instruction outside of the execute unit and the run-time execution process (col. 3: 12-17). The transformation is done by splitting of a hyper-block into two paths (col. 12: 25-30). Therefore it would have been obvious to one skilled in the art at the time of the invention was made to modify portion of the instruction at runtime to accelerate execution of a program by the

processor by transforming portions of said program code at run-time into the transformed instruction set architecture for more efficient execution and caching the transformed code within the instruction stream cache for possible repeated execution without requiring repeated transformations as once suggested by Wong (col. 36:10-19).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 12-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Moreno (US 5,951,674).

As per claim 12 (Currently Amended), Moreno discloses a multiprocessor system (e.g. FIG. 6 and related text), configured for operating with the process according to Claim 1, comprising:

a first processor having a given instruction set architecture and configured to execute programs with instruction words of a first length (e.g. FIG. 6, element 606 and related text);

a second processor having the given instruction set architecture and configured to execute programs with instruction words of a second length; (col. 19:14-20 "... FIG. 16 is ... processor unit 706 ...");

means for converting instruction words of the first length compiled for execution on the first processor into modified instruction words of the second length executable on the second processor (col. 13: 60-65 "... transforms large tree-instructions into variable-length VLIWs ... ").

As per claim 13 (Currently Amended), Moreno discloses the multiprocessor system according to claim 12, ~~characterized in that~~ wherein said processors are all of the VLIW type (e.g. FIG. 6, element 606 and related text).

As per claim 14 (Currently Amended), Moreno discloses the multiprocessor system according to claim 12, ~~characterized in that~~ wherein said plurality of processors comprises at

least one VLIW processor (e.g. FIG. 6, element 606 and related text) and at least one superscalar processor (col. 9:47-55 "... superscalar processors ...").

As per claim 15, Moreno discloses a system comprising:

a plurality of processors coupled for receiving instruction sets (e.g. FIG. 6, element 606, FIG. 16, element 706 and related text);

a first processor of the plurality coupled to each of the other processors within said plurality, said first processor receiving from the other processors data representative of the workload of each of said other processors (e.g. FIG. 6, element 606, FIG. 16, element 706 and related text);

an output signal from said first processor to said instruction set stream, said output signal controlling the instructions, which are sent to each of said processors based on the results of the workload measurement of said processors (e.g. FIG. 6, element 606 and related text).

As per claim 16, Moreno discloses the system according to claim 15, wherein said workload measurement comprises power consumption of each of said processors of said plurality (col. 9:47-55 "... superscalar processors ...").

As per claim 17, Moreno discloses the system according to claim 15, wherein said workload measurement comprises memory usage of each of said processors of said plurality (e.g. FIG. 5, element 501 and related text).

As per claim 18, Moreno discloses the system according to claim 15, wherein said workload measurement comprises number of operations carried out by each of said processors of said plurality (e.g. FIG. 5, element 501 and related text).

As per claim 19, Moreno discloses a process of directing instruction sets to be executed by a plurality of processors in a system comprising:

receiving a plurality of instruction sets on a bus line connected to said processors (e.g. Fig. 6, element 616 and related text);

receiving workload data at a first processor of said plurality of processors, said workload data being representative of workload of each of the processors of said plurality (e.g. Fig. 6, element 612 and related text);

comparing the workload of each of the processors (e.g. Fig. 11and related text); and

sending a signal from said first processor based on the data representative of the workload of each of the processors of said plurality to the bus line for modifying the number of instruction sets sent to each processor based on their respective workloads (e.g. Fig. 14 and related text).

As per claim 20, Moreno discloses the process according to claim 19, wherein said workload data includes data regarding power consumption of each of said processors of said plurality (e.g. FIG. 5, element 501 and related text).

As per claim 21, Moreno discloses the system according to claim 19, wherein said workload data includes data regarding memory usage of each of said processors of said plurality (in column 23, lines 50-55 "... maximum address size of the target processor...").

As per claim 22, Moreno discloses the system according to claim 19, wherein said workload data includes data regarding the number of operations carried out by each of said processors of said plurality (col. 9:47-55 "... superscalar processors ...").

Response to Arguments

9. Applicant's arguments with respect to claims 1-22 and 26-27 have been considered but are moot in view of the new ground(s) of rejection. See art made of record Moreno et al. (US 5,951,674 B1) and Wong (US 6,988,183 B1).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isaac T. Tecklu whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Isaac Tecklu
Art Unit 2192

TUAN DAM
SUPERVISORY PATENT EXAMINER